IFW

Docket No.: 071971-0015 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Shiro SAKIYAMA, et al.	:	Confirmation Number: 6689
Application No.: 10/511,165	:	Group Art Unit: 2816
Filed: October 14, 2004	:	Examiner: HILTUNEN, THOMAS J

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH REDUCED SPEED VARIATIONS

REQUEST FOR CORRECTED FILING RECEIPT

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that **the number of claims listed on the official filing receipt is incorrect. Attached is a copy of the Preliminary Amendment, which evidences that the number of claims should now be: 2 independent claims and 9 dependent claims totaling 11 claims.** It is requested that a corrected filing receipt be issued.

Respectfully submitted,

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APPL NO.	FILING OR 371(c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	TOT CLMS	IND CLMS
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CONFIRMATION NO. 6689

20277
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600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

CORRECTED FILING RECEIPT

OC000000024721304

Date Mailed: 07/09/2007

Receipt is acknowledged of this nonprovisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number **20277**.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/01942 02/19/2004

Foreign Applications

JAPAN 2003-047418 02/25/2003

If Required, Foreign Filing License Granted: 09/22/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US10/511,165

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor integrated circuit with reduced speed variations

Preliminary Class

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AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-5. (Cancelled)

6. (Previously presented) A semiconductor integrated circuit, comprising:

a main circuit including a plurality of MOS transistors of a MOS structure in which a source potential and a substrate potential are separated from each other, and operating while receiving a predetermined operating power supply voltage; and

a substrate potential control circuit for controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value that is sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit, the substrate potential control circuit, including:

a constant current generation circuit;

a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value; and

a differential amplifier circuit for controlling a substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit,

wherein the substrate potential control circuit controls the substrate potential of each of the MOS transistors in the main circuit so that the substrate potential is equal to the substrate potential of the current-voltage conversion circuit controlled by the differential amplifier circuit.

7. (Original) The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is proportional to the operating power supply voltage value within the operating voltage range.

8. (Original) The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range.

9. (Original) The semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges;

the constant current value of the constant current generation circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit; and

the linear function relationship between the constant current value of the constant current generation circuit and the operating power supply voltage value is different for each operating power supply voltage range.

10. (Original) The semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a plurality of constant current values, and selectively outputs one of the plurality of constant current values.

11. (Original) The semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the actual saturation current value of the MOS transistors of the main circuit.

12. (Original) The semiconductor integrated circuit of claim 11, wherein the constant current generation circuit includes an adjustment circuit for reducing variations in the generated constant current value.

13. (Previously presented) A semiconductor integrated circuit, comprising:

a main circuit including a plurality of MOS transistors of a MOS structure, and operating while receiving an operating power supply voltage; and

a power supply voltage control circuit for controlling the operating power supply voltage supplied to the main circuit, wherein:

a target saturation current value of the MOS transistors that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage, is set in the power supply voltage control circuit; and

the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value.

14. (Original) The semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is a target saturation current value of an nMOS transistor or that of a pMOS transistor from among the MOS transistors of the main circuit, or is an average value between the target saturation current values of the nMOS and pMOS transistors.

15. (Previously Presented) The semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage supplied to the main circuit.

16. (Previously Presented) The semiconductor integrated circuit of claim 13, wherein:

the main circuit includes a plurality of operating power supply voltage ranges;

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit;

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range.